Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. CLR**
2. **CLK**
3. **A**
4. **B**
5. **C**
6. **D**
7. **ENP**
8. **GND**
9. **N. LOAD**
10. **ENT**
11. **QD**
12. **QC**
13. **QB**
14. **QA**
15. **VCC**

**.084”**

**.074”**

**2 1 16 15**

**8 9 10**

**14**

**13**

**12**

**11**

**3**

**4**

**5**

**6**

**7**

**LS**

**163**

**C**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS163C**

**APPROVED BY: DK DIE SIZE .074” X .084” DATE: 8/29/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: 54LS163A**

**DG 10.1.2**

#### Rev B, 7/19/02